An Internally Matched LTCC 3G W-CDMA 180 Watt LDMOS Power Amplifier

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ABSTRACT — **A wide band CDMA LDMOS power transistor, with internal RF matching and bias networks, fabricated on LTCC (Low Temperature Cofired Ceramic) substrates, has been developed. The internally matched packaged device can be configured to deliver output power of 180 watts, while providing third order inter-modulation distortion products less than -40 dBc, 20 % efficiency, and 12 dB of gain. The terminal impedances of the packaged LDMOS transistor, at the gate and drain leads respectively, are greater than 5 W. The LTCC elements each contain embedded passive L-C circuitry, forming the input and output matching networks. These networks are designed to transform to a high level of impedance, to the source and load impedance targets required by the devices in order to achieve optimal wide band CDMA performance.**

I. INTRODUCTION

The current method of internally matching high power transistors to reasonable impedance levels usually employs the use of wire bonds and MOS capacitors, which is a complex and expensive process. This paper presents an improved high power transistor package where the matching elements are embedded in LTCC substrate resulting in a simple low cost highly reliable package.

II. *MATCHING NETWORK DESIGN*

The LTCC input and output matching networks are synthesized in such a manner, as to provide the proper terminating impedances for the LDMOS die at the fundamental, second and third harmonic frequencies of the 2.14 GHz WCDMA band. In addition to providing optimum impedance matching with a RF short at the 2nd harmonic, the network also provides DC bias paths from the package leads to the gate and drain of each die. The matching networks provide a high impedance transformation ratio yielding an impedance in excess of 5 Ω at the leads of the transistor package.

Load impedance target values for the LTCC network designs are determined using load pull measurements of the active device in test packages and through nonlinear simulation techniques. The device is operated with a quiescent drain current of 1500 mA and the load is tuned to provide optimum power output, gain, efficiency, and minimum inter-modulation (IMD) distortion products. The tuned impedance values at the fundamental, 2nd and 3rd harmonics are then used as the design targets for the LTCC networks. The impedance values measured using the load pull system are taken at the transistor package reference plane and therefore must be de-embedded back to the active device reference plane before they can be used to design the LTCC matching networks. The impedance at the drain reference plane, is determined using a circuit model of the transistor test package and test fixture. Device source and load impedance targets are then

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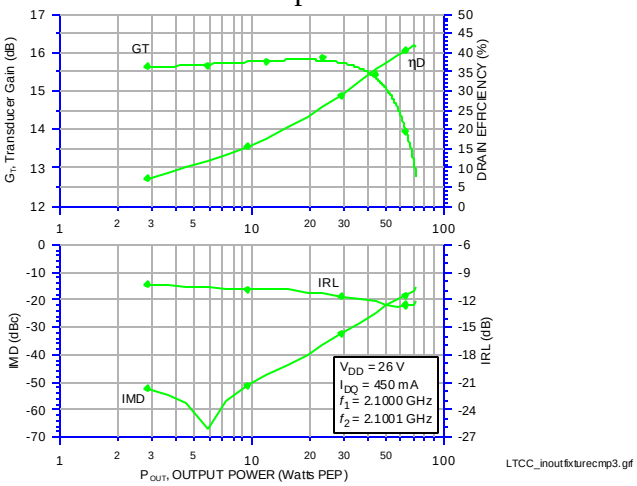
determined at the fundamental frequency as well as at the second and third harmonic frequencies. Once these target impedances are known, LTCC matching networks can be synthesized using a combination of circuit analysis and electromagnetic field simulation and optimization.

Low pass network topologies were selected for both the input and output matching circuits. Two sections are required to transform the low device impedance up to the 5 Ω level while still providing greater than the 60 MHz of bandwidth required for WCDMA operation. Wire bonds, as well as helical transmission lines, which are embedded in the LTCC structure, are used to form series inductive elements. Shunt capacitive elements, are formed by fabricating multi-layer parallel plate structures within the LTCC substrate.

The network synthesis was conducted in a conventional manner. The input and output networks were first realized with ideal elements; unfortunately, transmission line elements embedded in ceramic loaded stripline hardly appear ideal. Inductive as well as capacitive elements exhibit high associated parasitics. Hence, circuit synthesis and circuit optimization, must be performed by employing an EM solver. LTCC structures traditionally have many layers and these layers, for means of analysis, can be quite different in thickness. Because of the large range in dimensions and large number of layers, a full wave EM simulator was used for electromagnetic analysis. In addition, the realization of LTCC networks is much more complex than just accounting for parasitics since the high degree of coupling found in and between the individual capacitor and inductor structures, render conventional simple lumped element models useless.

III. PACKAGED TRANSISTOR PERFORMANCE

The packaged transistor consists of LTCC matching networks and LDMOS transistor die. These devices and circuits are assembled onto the package ground flange and multiple wire bonds are added to connect the die to the LTCC networks. The power output and efficiency performance of one set of matching networks and a single device is shown in Figure 1. The top portion of the figure shows amplifier efficiency and transducer gain as a function of output power in Watts. The bottom portion of the figure illustrates IMD (third-order) and input return loss for the packaged device. As can be seen from the figure shown below, the performance of the amplifier section is well suited for wide band CDMA operation.



IV. CONCLUSION

The LTCC matching network method illustrated above can be extended to produce internally matched transistors, for power amplifier applications. The matching networks are low cost and exhibit very low loss, excellent repeatability, and can be integrated into the package lead frame assembly.

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